Logic Gates and Ladder Diagrams

Symbols for Common and Ladder Logic Elements

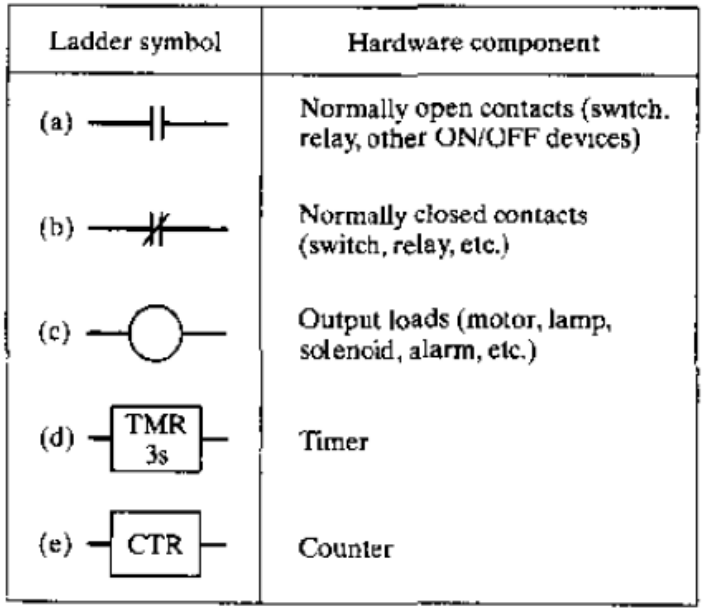
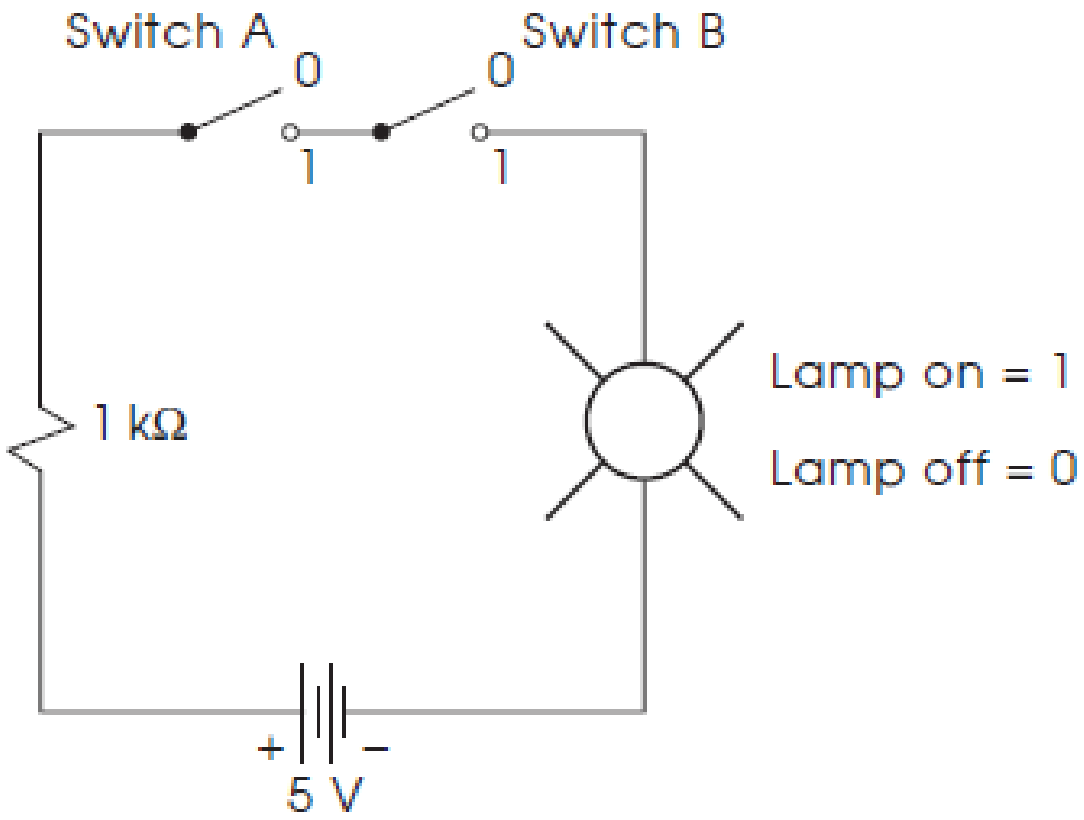


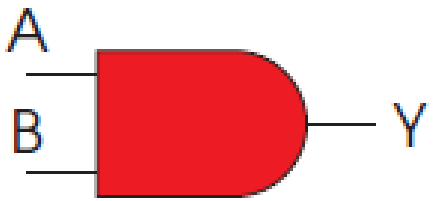
Figure 8.8 Symbols for common logic and sequence elements used in ladder logic diagrams.

AND Gate



AND Gate

Boolean expression: $Y = A \cdot B$

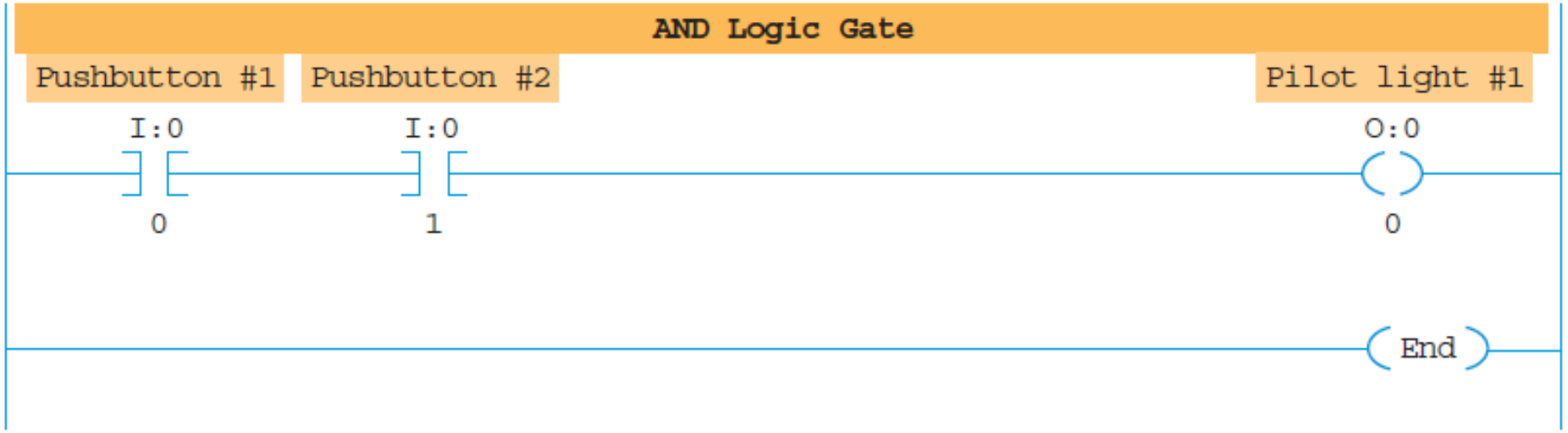


Two-input AND gate

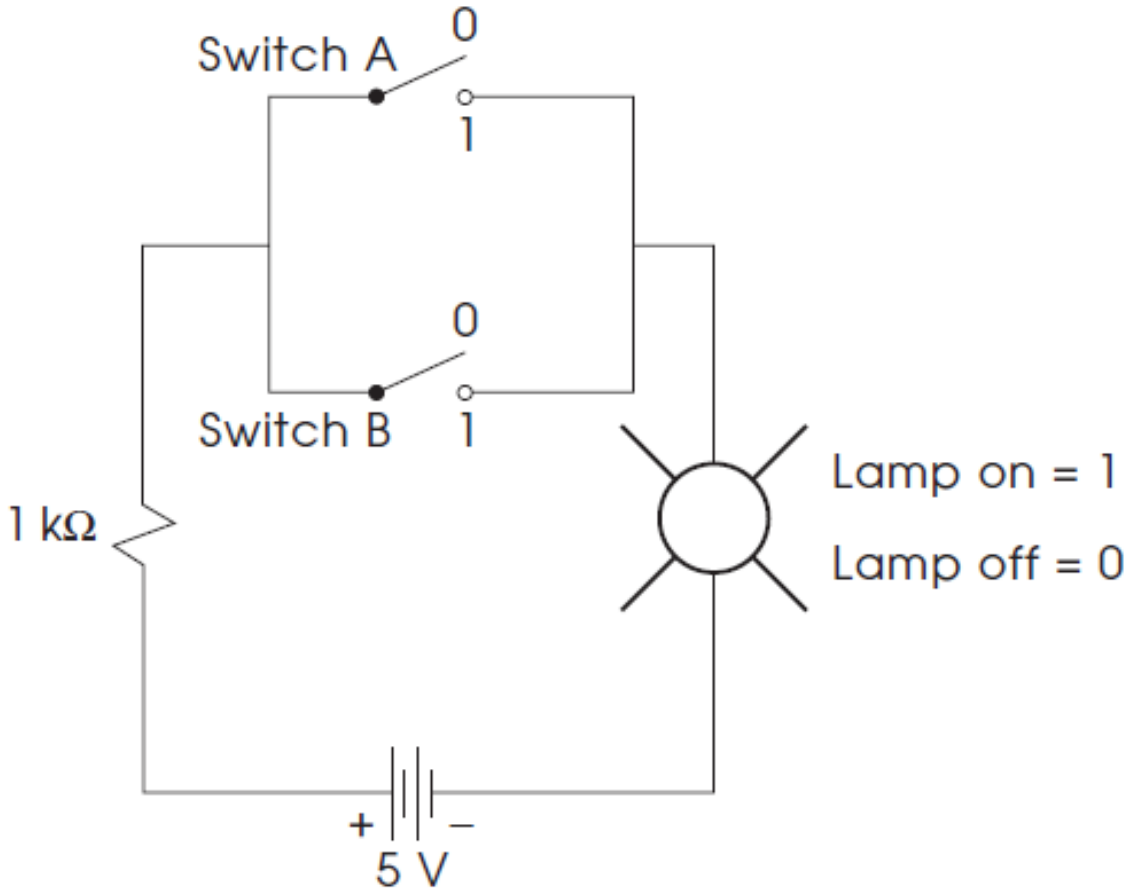
A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1

Truth table

AND Gate

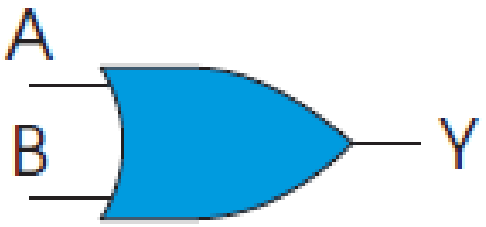

AND Logic Gate
Pushbutton #1
Pushbutton #2
Pilot light #1
I:0
I:0
O:0
0
1
0
End

OR Gate



OR Gate

Boolean expression: Y = A + B

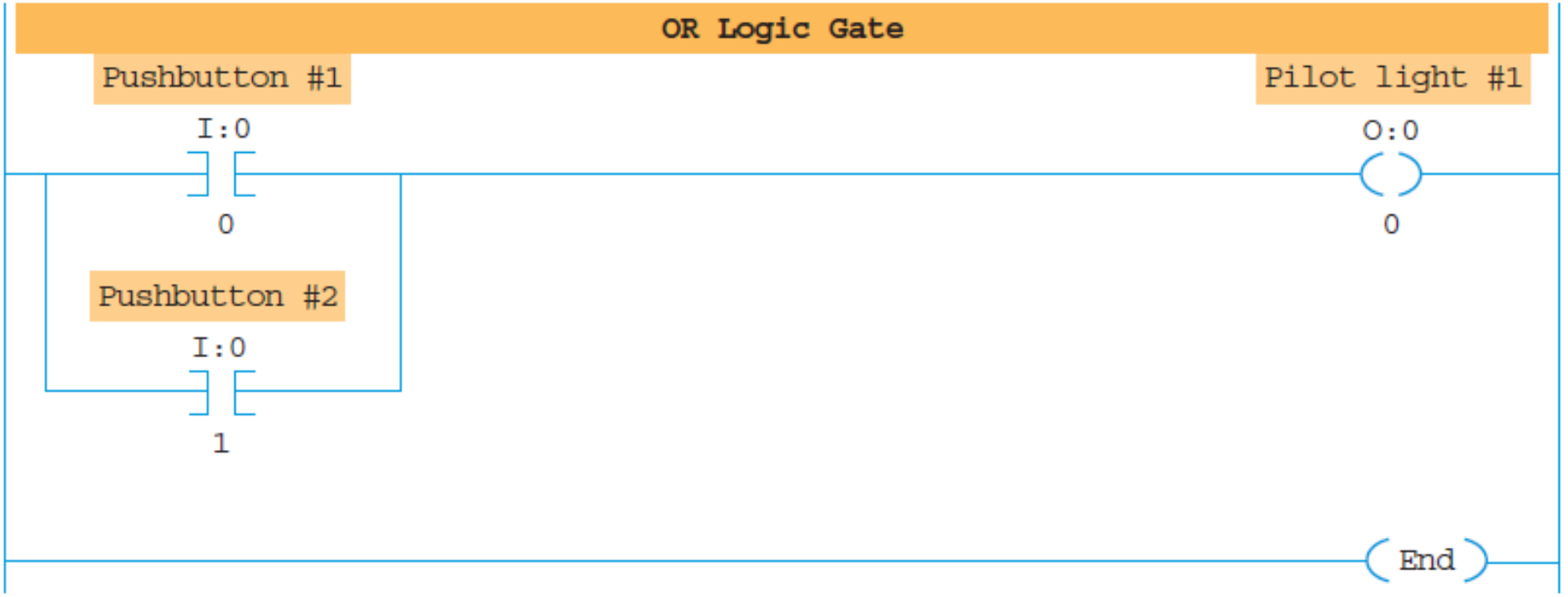


Two-input OR gate

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	1

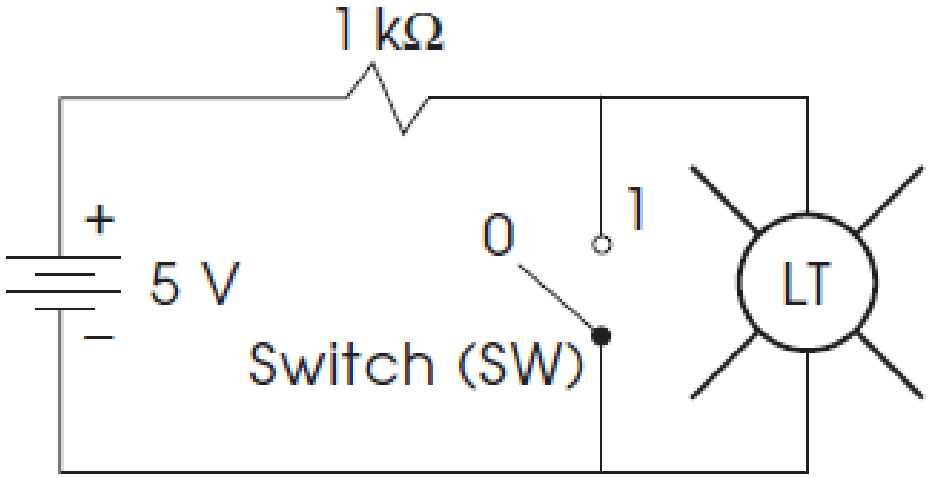
Truth table

OR Gate


OR Logic Gate
Pushbutton #1
I:0
0
Pushbutton #2
I:0
1
Pilot light #1
O:0
0
End

NOT Gate

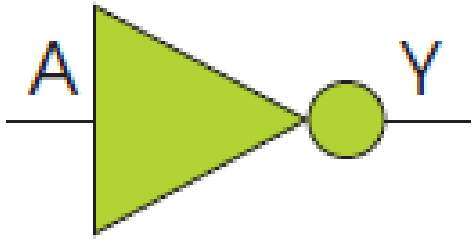
- **The output of a NOT gate is the inverse of the input.**
- **The NOT gate is sometimes called an inverter.**



Electric circuit emulating the function of a NOT gate.

NOT Gate

Boolean expression: $Y = A'$



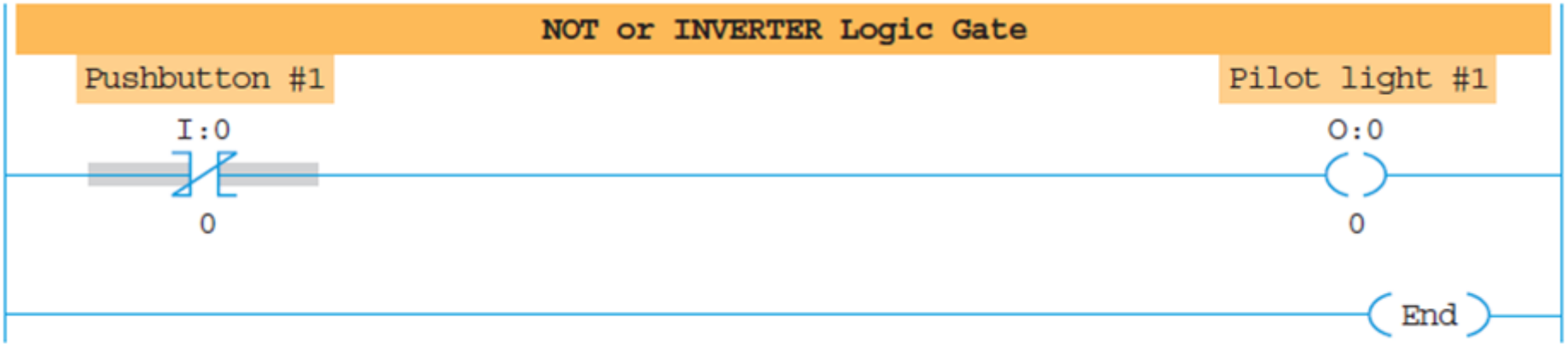
NOT gate symbol

A	Y
0	1
1	0

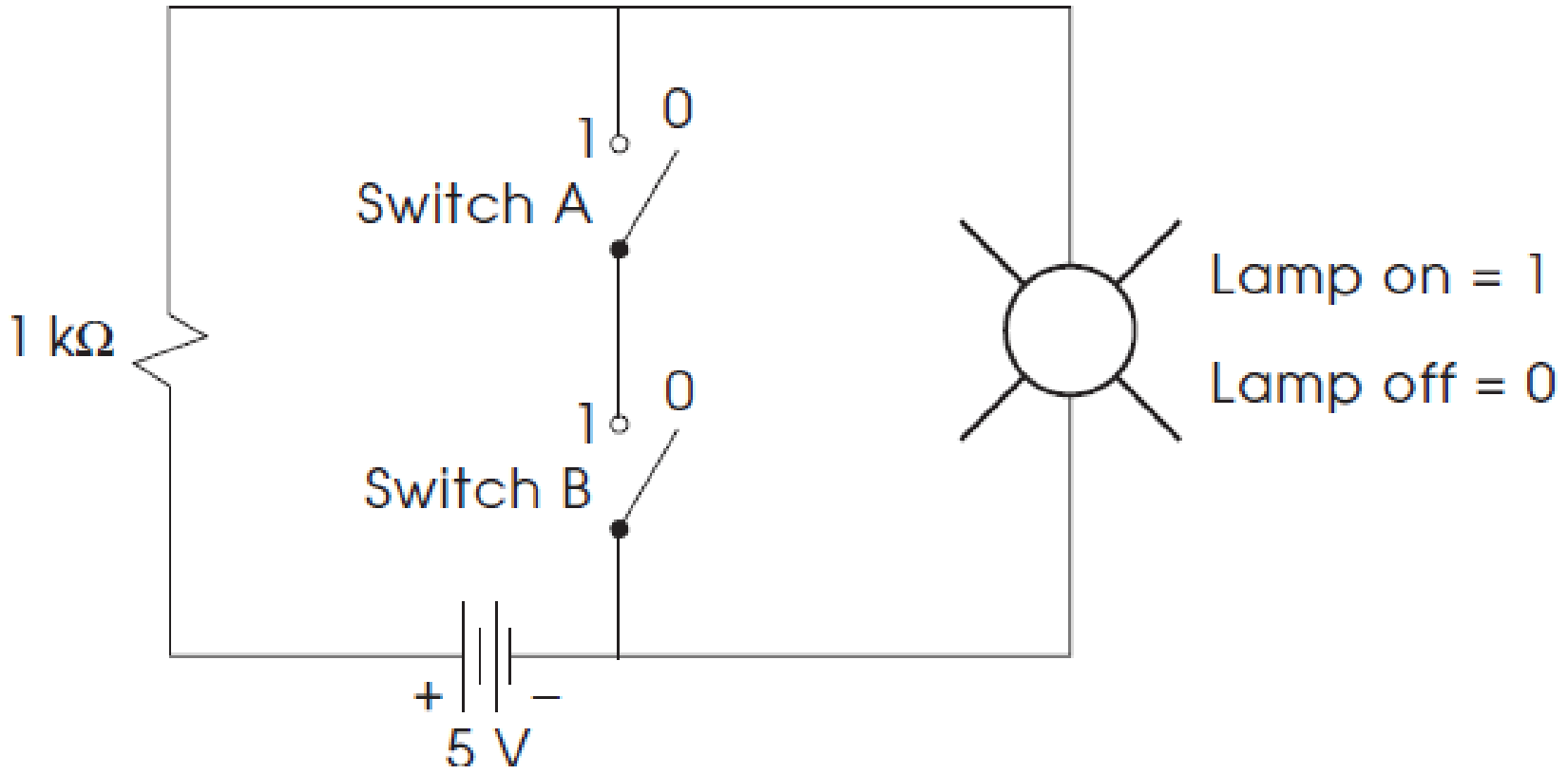
Truth table

Boolean expression, gate symbol, and truth table for NOT logic gate.

NOT Gate

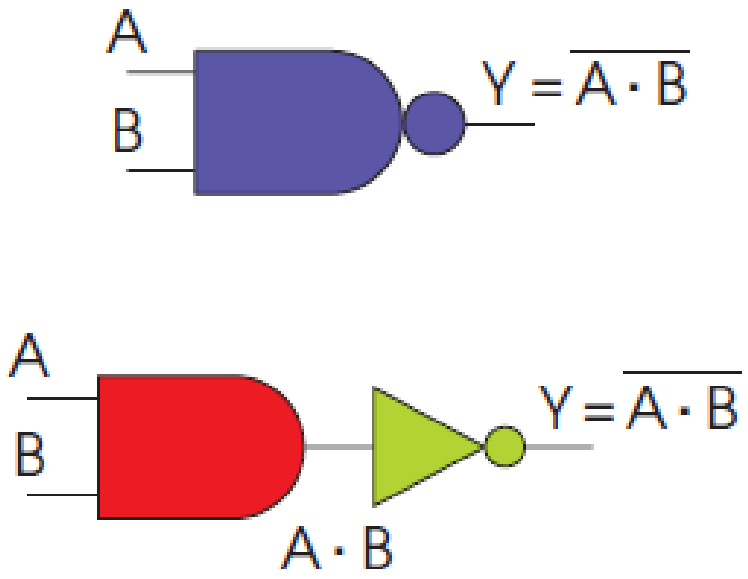

NOT or INVERTER Logic Gate
Pushbutton #1
I:0
0
Pilot light #1
O:0
0
End

NAND (NOT AND) Gate



NAND (NOT AND) Gate

Boolean expression: $Y = \overline{A \cdot B} = \overline{A} + \overline{B}$

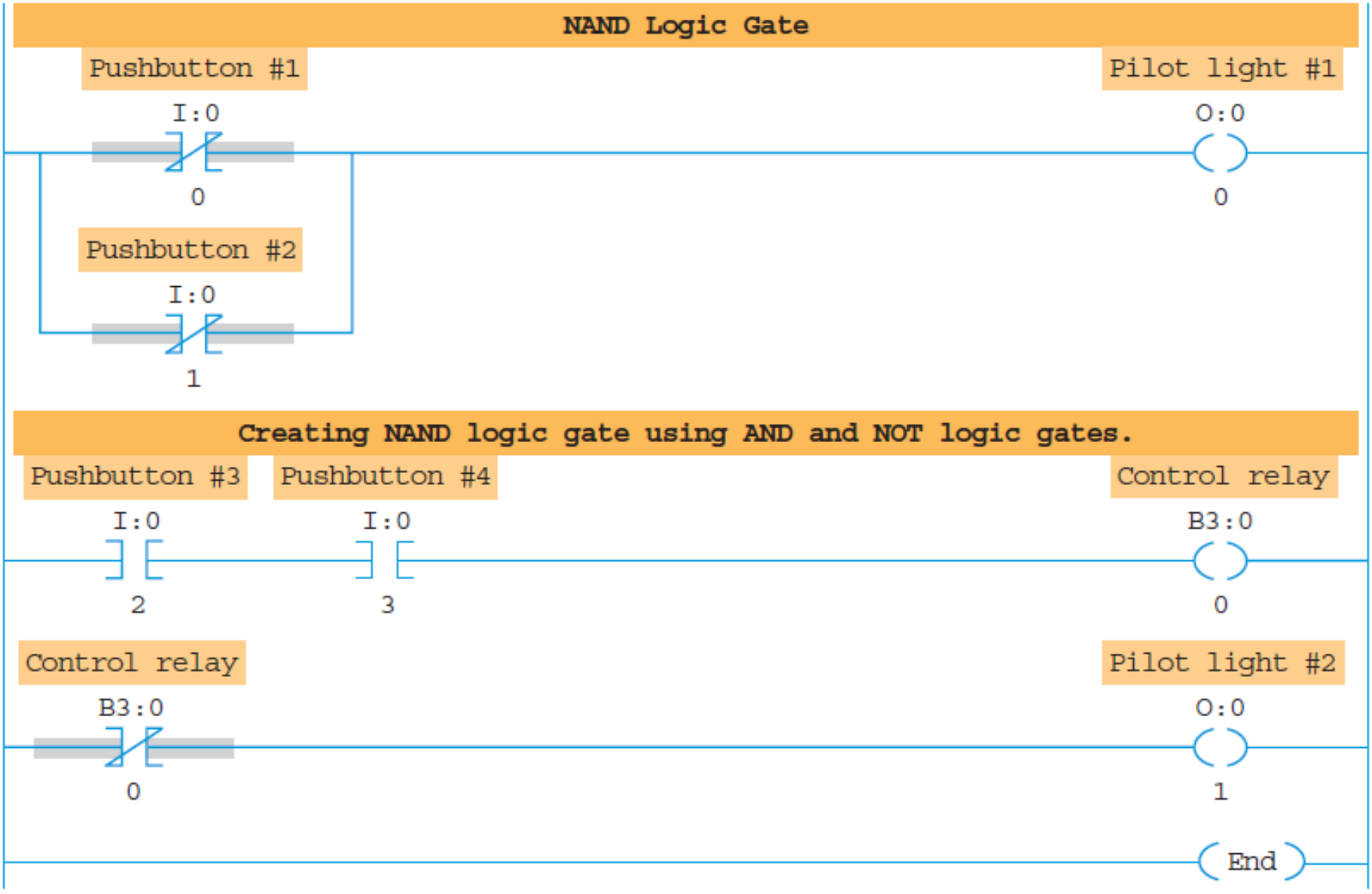


NAND gate

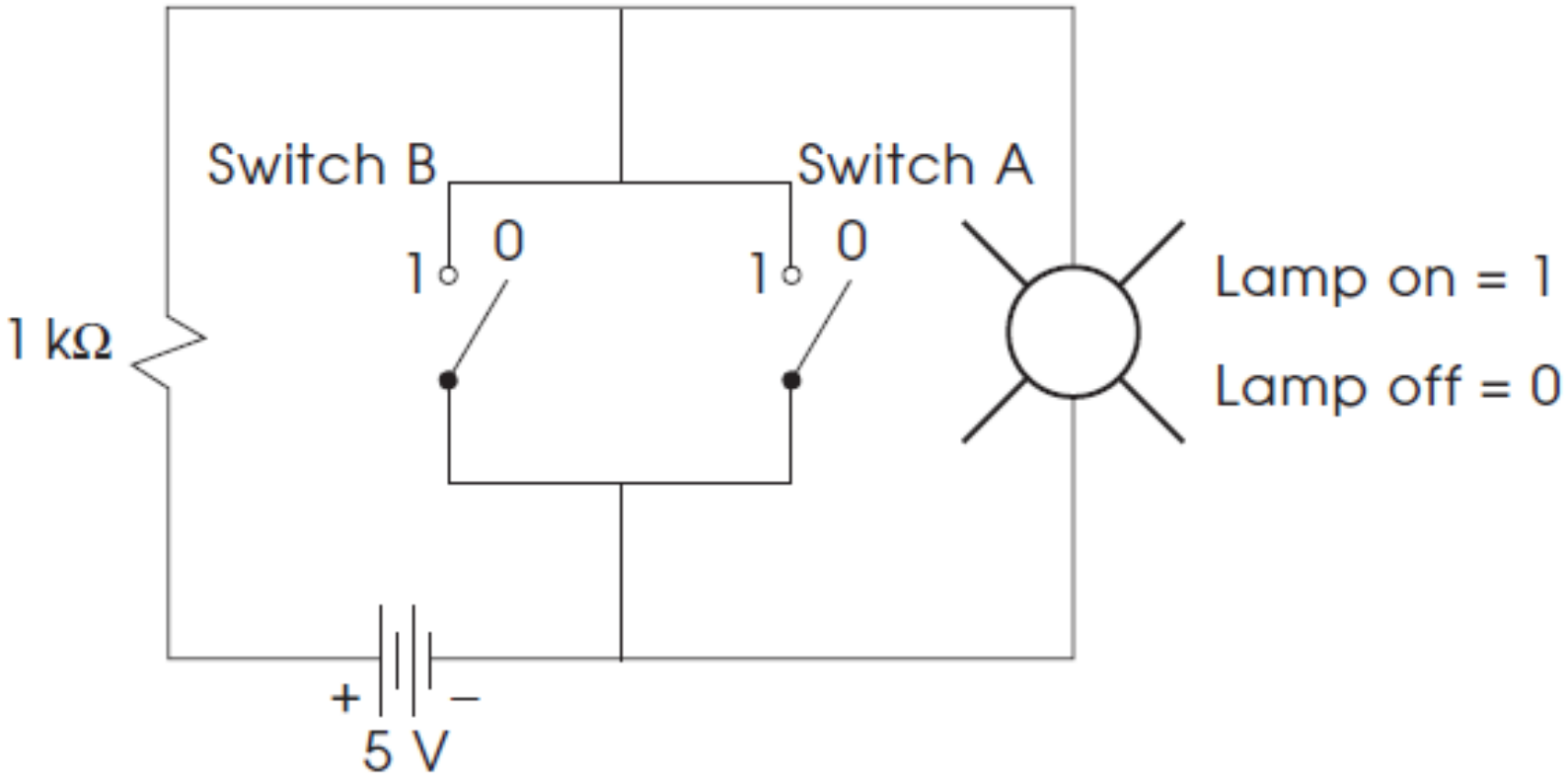
A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

Truth table

NAND (NOT AND) Gate

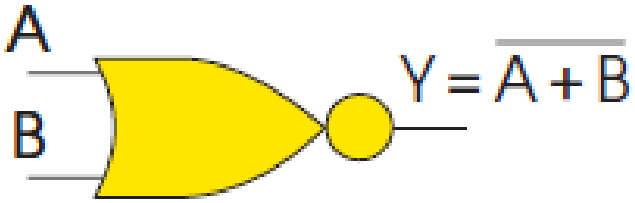


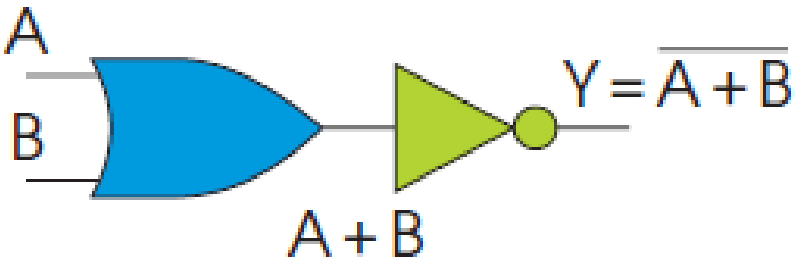
NOR (NOT OR) Gate



NOR (NOT OR) Gate

Boolean expression: $Y = \overline{A + B} = \overline{A} \cdot \overline{B}$



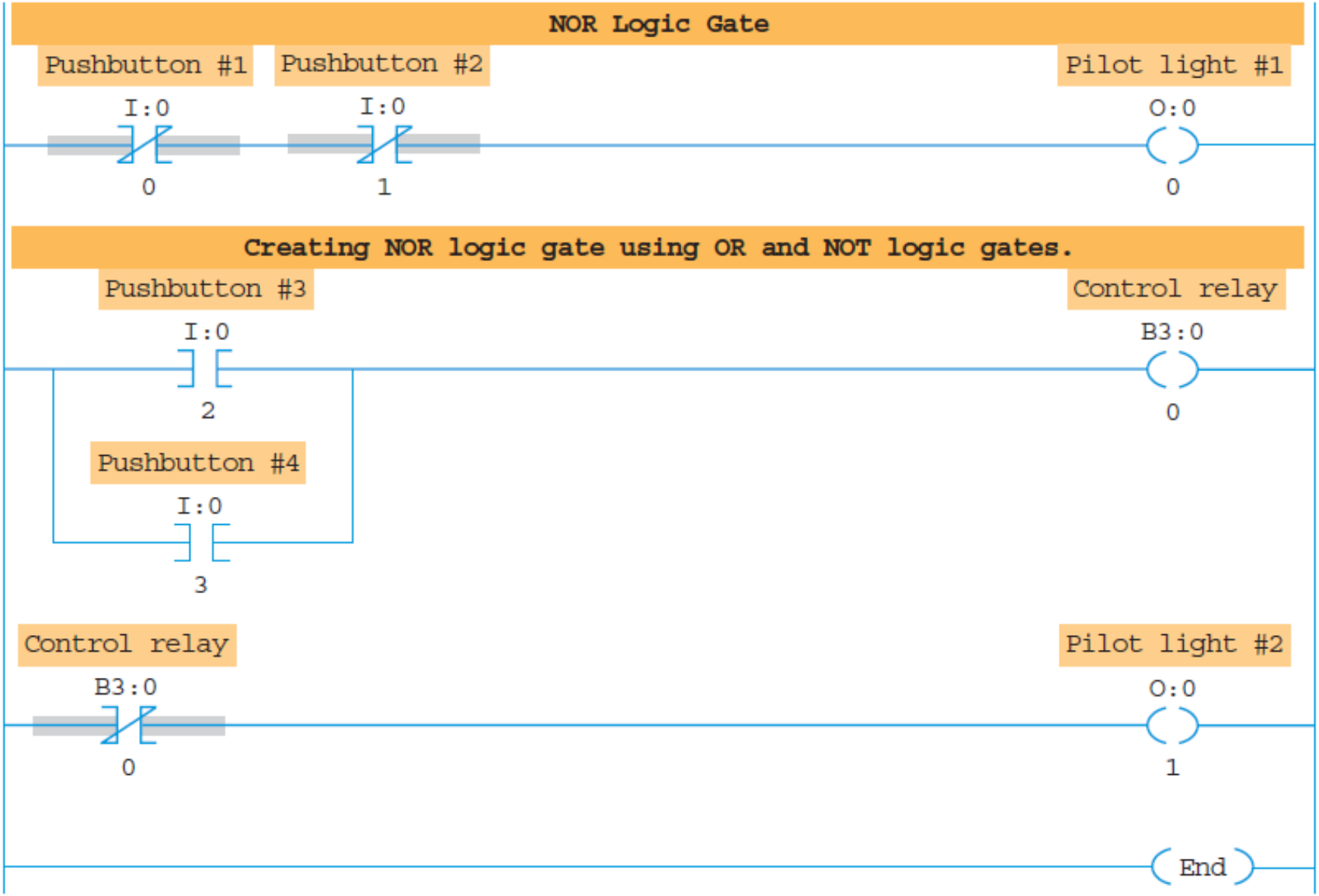


NOR gate

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

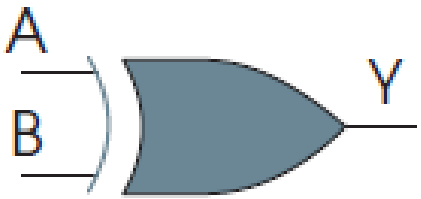
Truth table

NOR (NOT OR) Gate



XOR (Exclusive OR) Gate

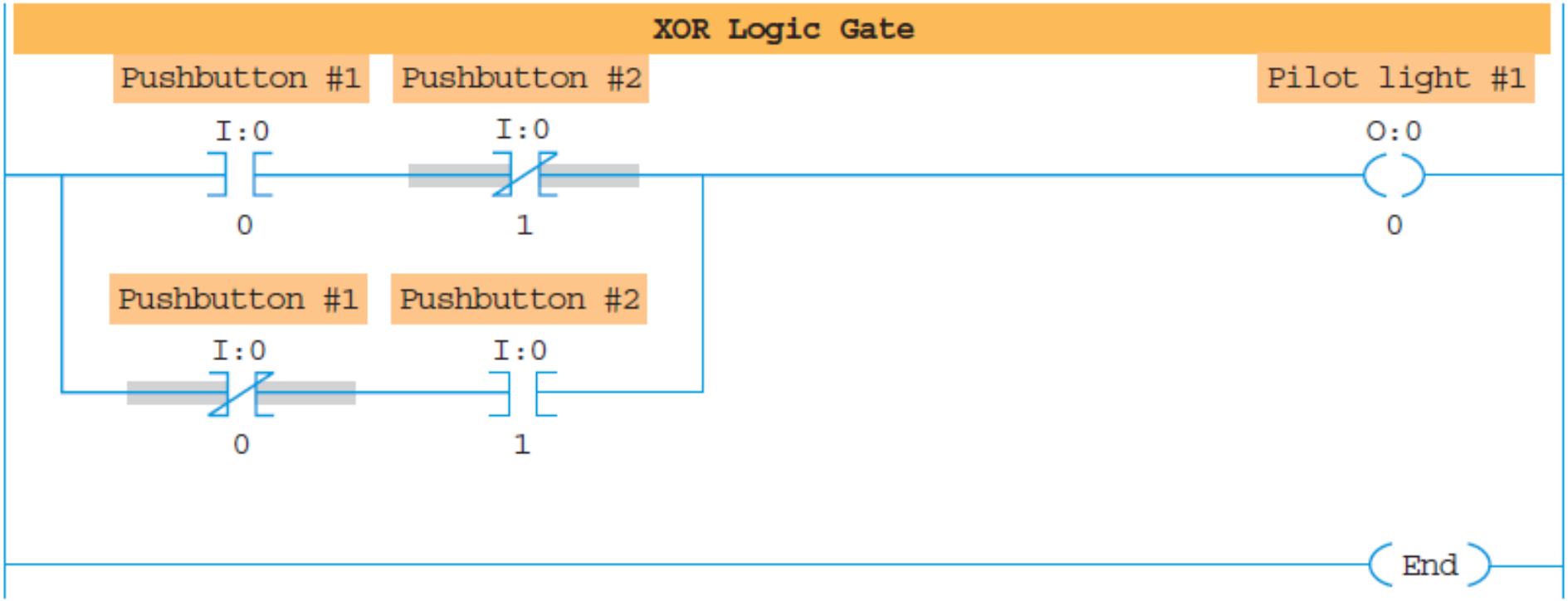
Boolean expression: $Y = A \oplus B = A \cdot \overline{B} + \overline{A} \cdot B$



XOR gate

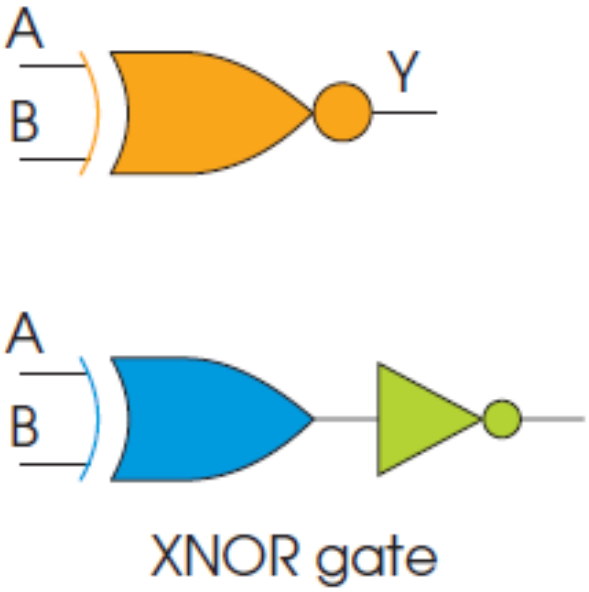
A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

XOR (Exclusive OR) Gate



XNOR (Exclusive NOR) Gate

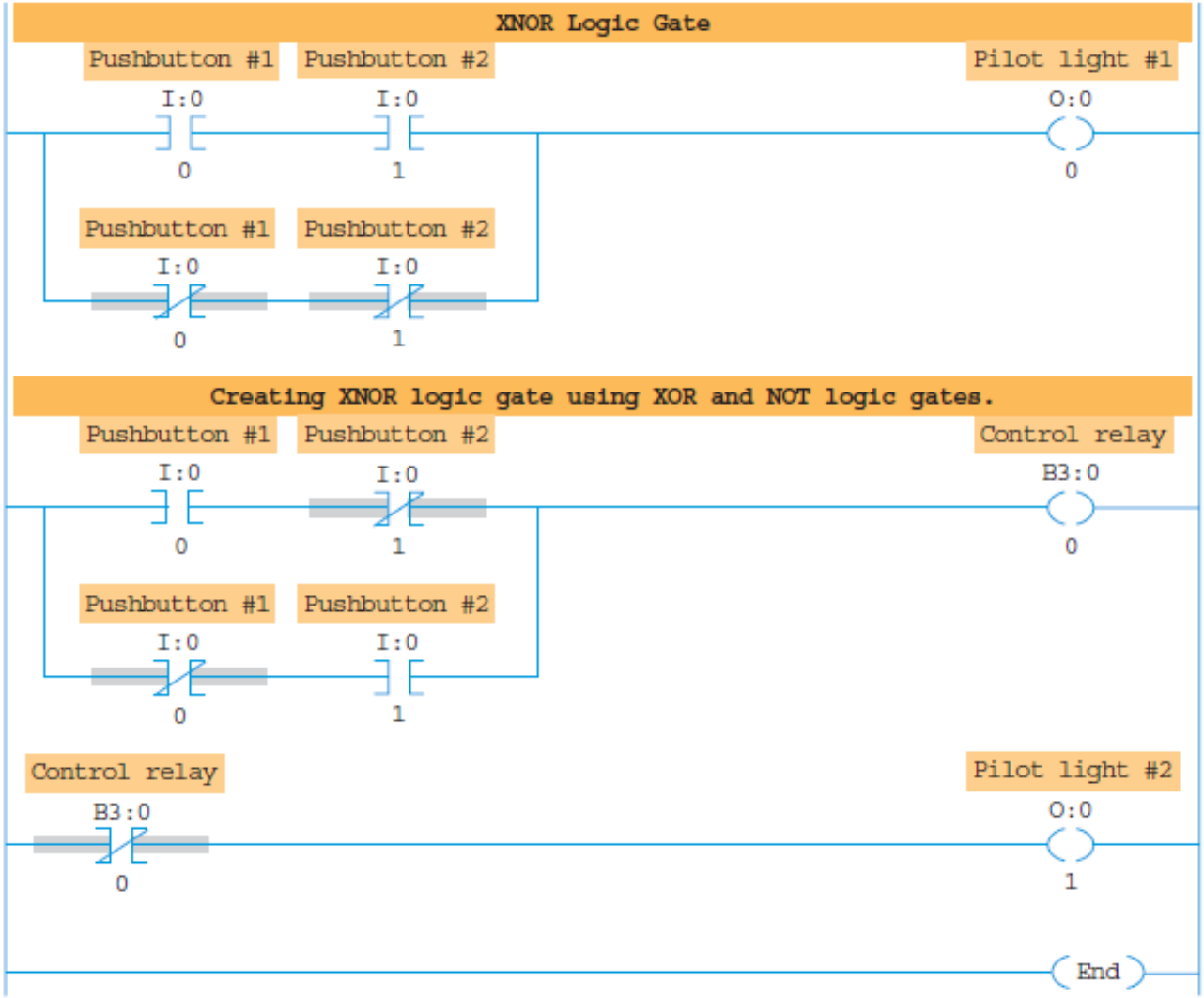
Boolean expression: $Y = \overline{A \oplus B} = A \cdot B + \overline{A} \cdot \overline{B}$



XNOR gate

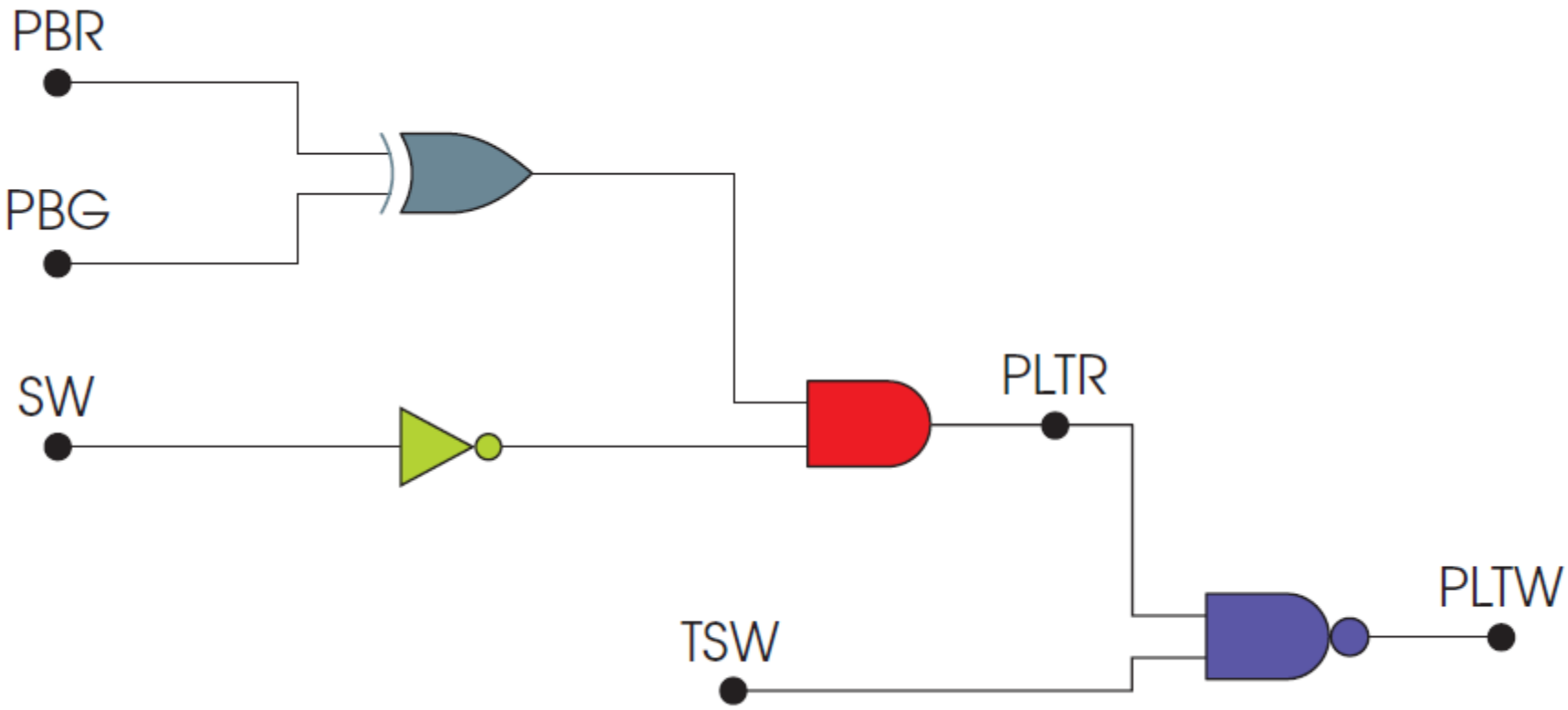
A	B	Y
0	0	1
0	1	0
1	0	0
1	1	1

XNOR (Exclusive NOR) Gate

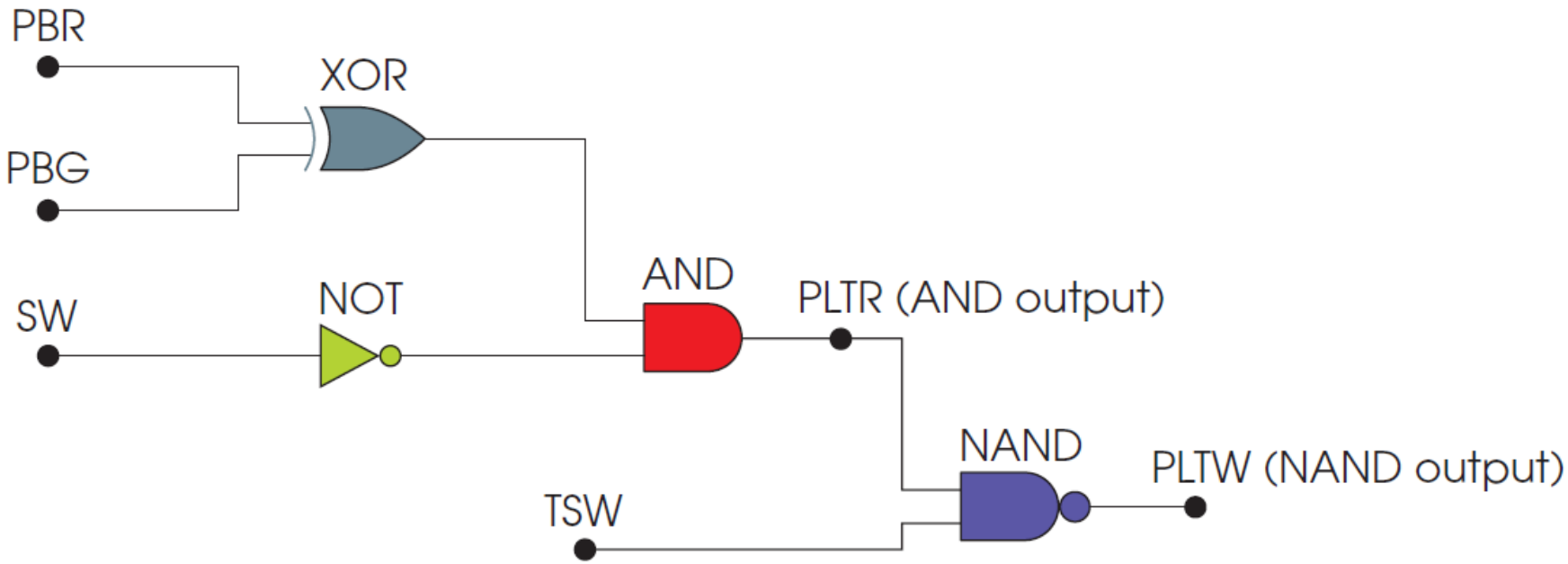


Creating PLC Ladder Logic Diagrams from Logic Gate Circuits

Problem 1

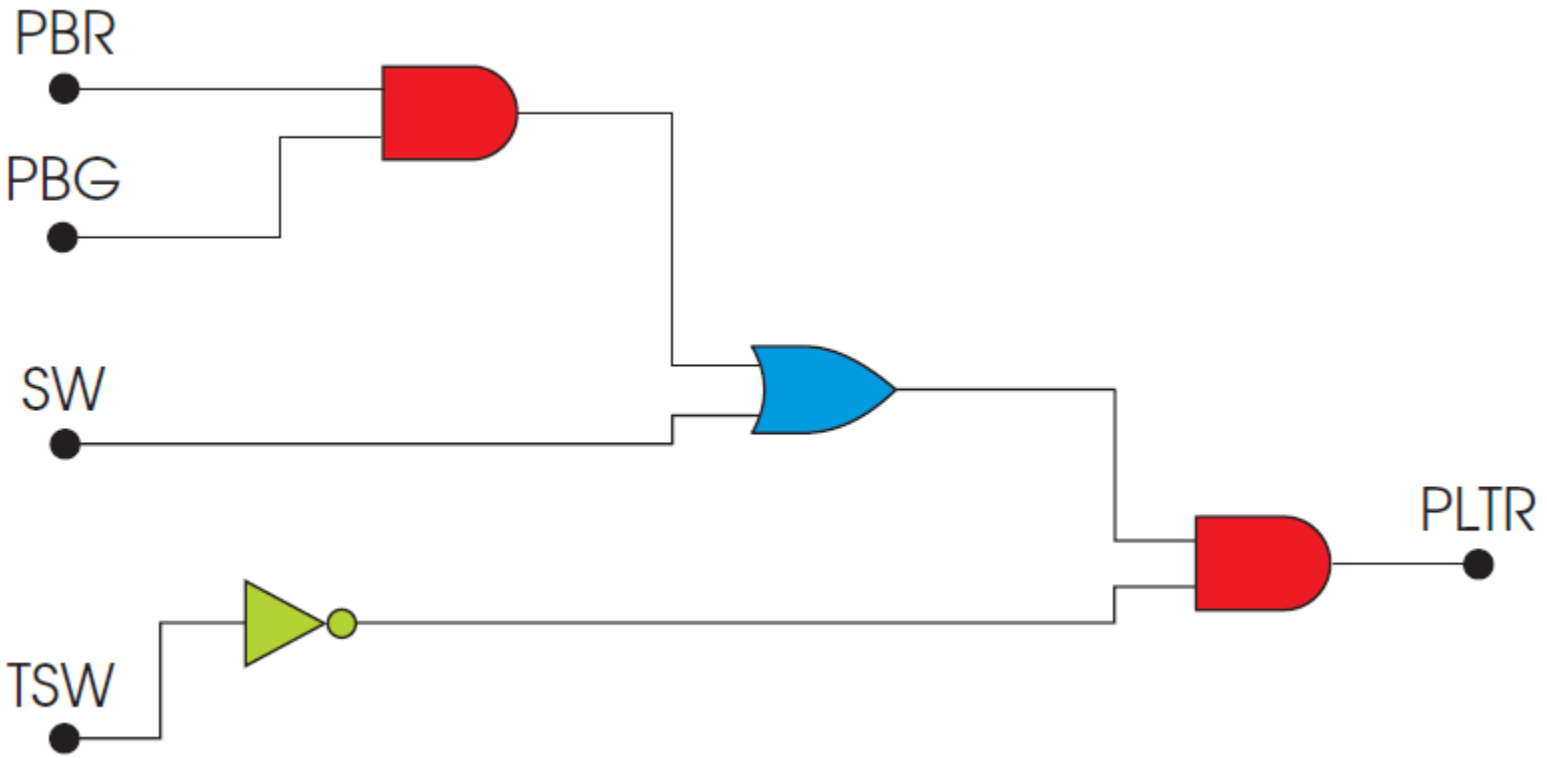


Creating PLC Ladder Logic Diagrams from Logic Gate Circuits



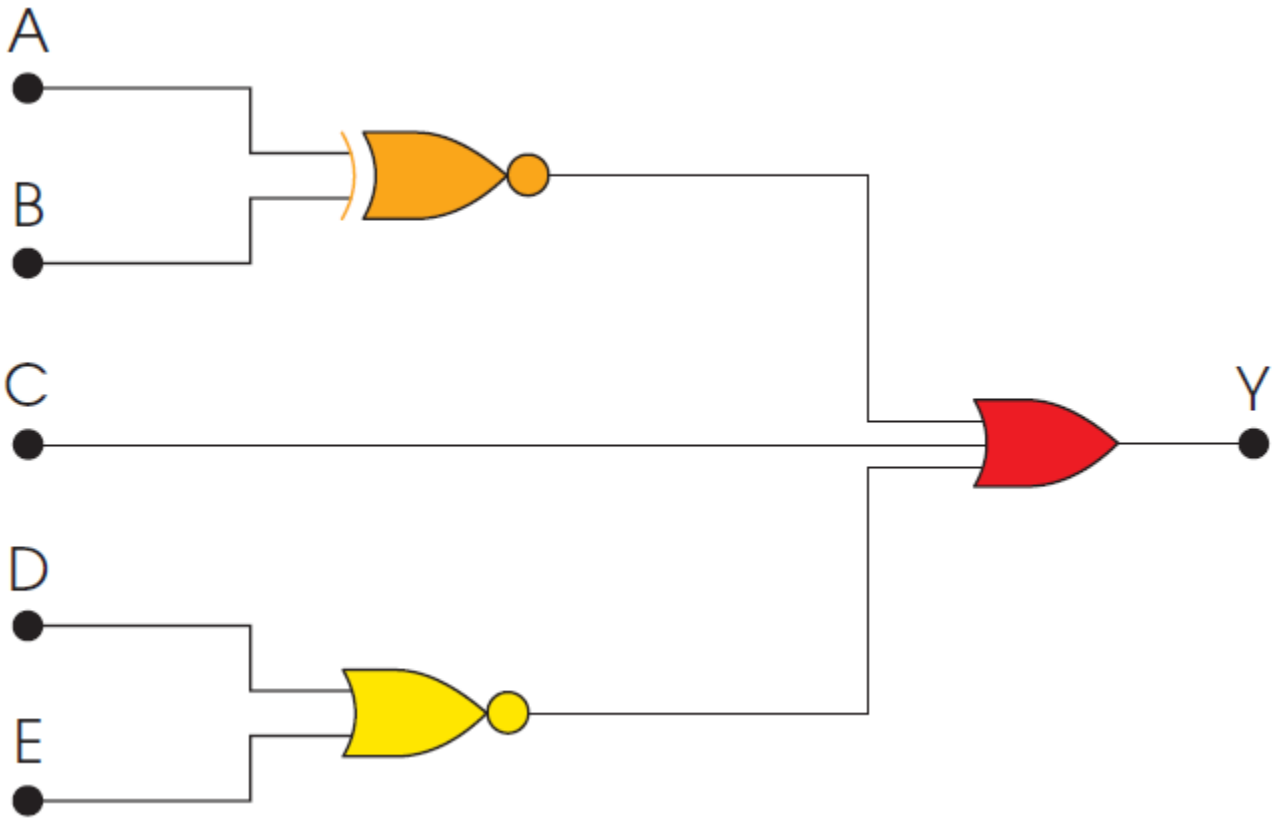
Creating PLC Ladder Logic Diagrams from Logic Gate Circuits

Problem 2

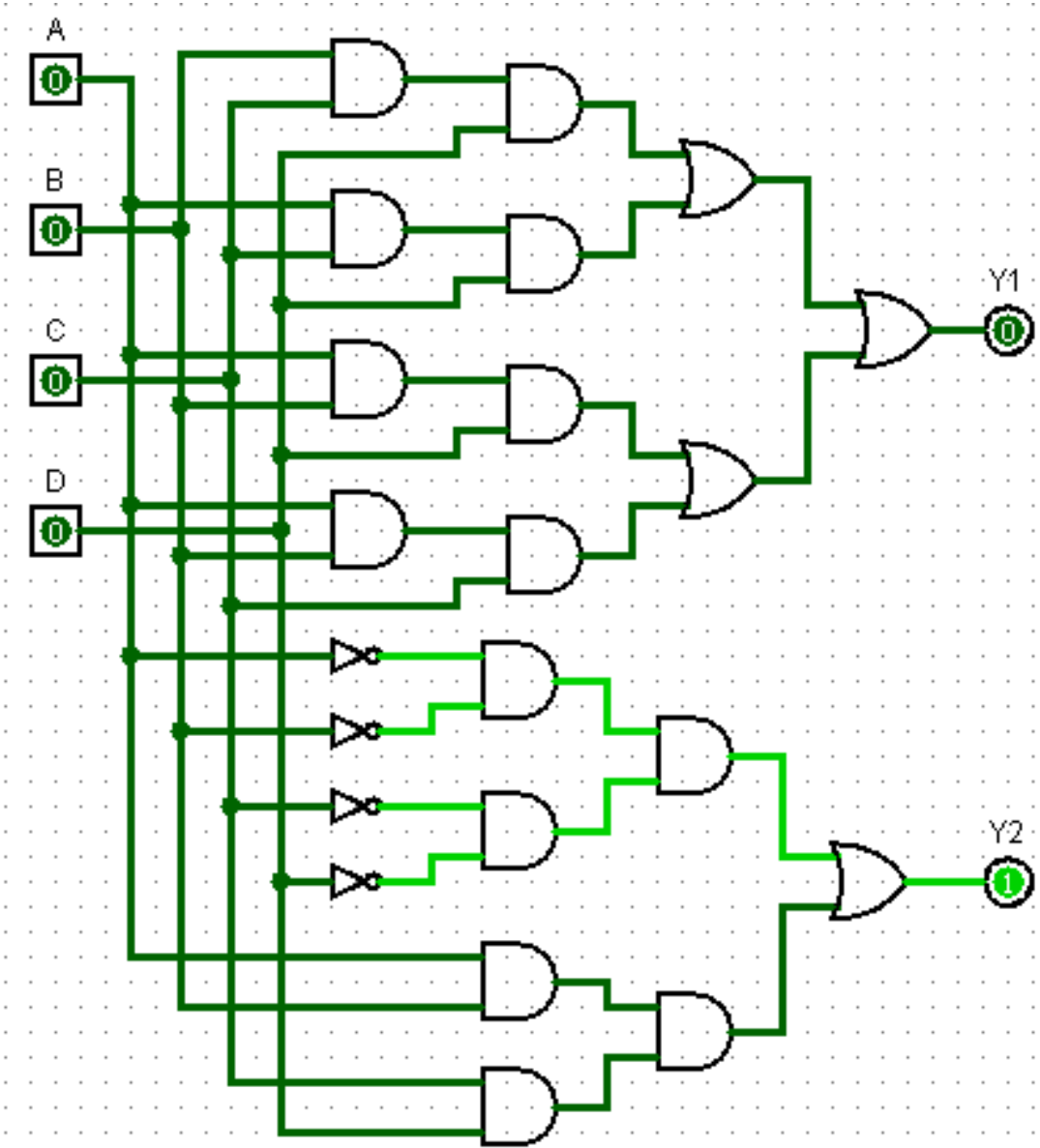


Creating PLC Ladder Logic Diagrams from Logic Gate Circuits

Problem 3



Solve It



Creating PLC Ladder Logic Diagrams from Boolean Expressions

Create the PLC ladder logic diagram for the following Boolean expressions.

1. $Y = A' + B + CD + EB$
2. $Y = (AB)' + AC + BC$
3. $Y = (A + B) \cdot (C + D)$

Boolean Algebra

COMMUTATIVE LAW

$$A + B = B + A$$

$$A \cdot B = B \cdot A$$

ASSOCIATIVE LAW

$$(A + B) + C = A + (B + C)$$

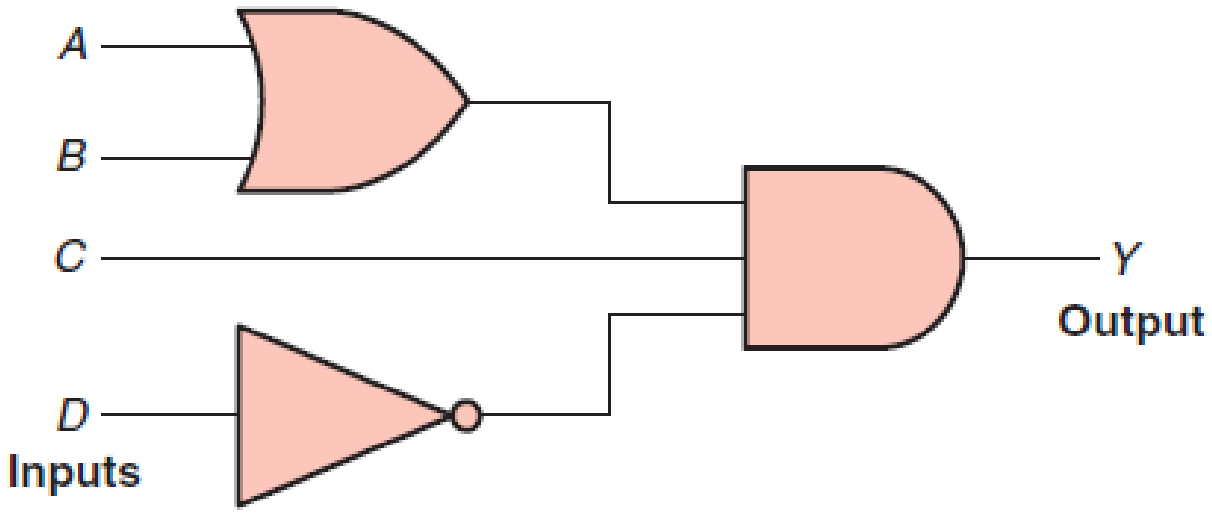
$$(A \cdot B) \cdot C = A \cdot (B \cdot C)$$

DISTRIBUTIVE LAW

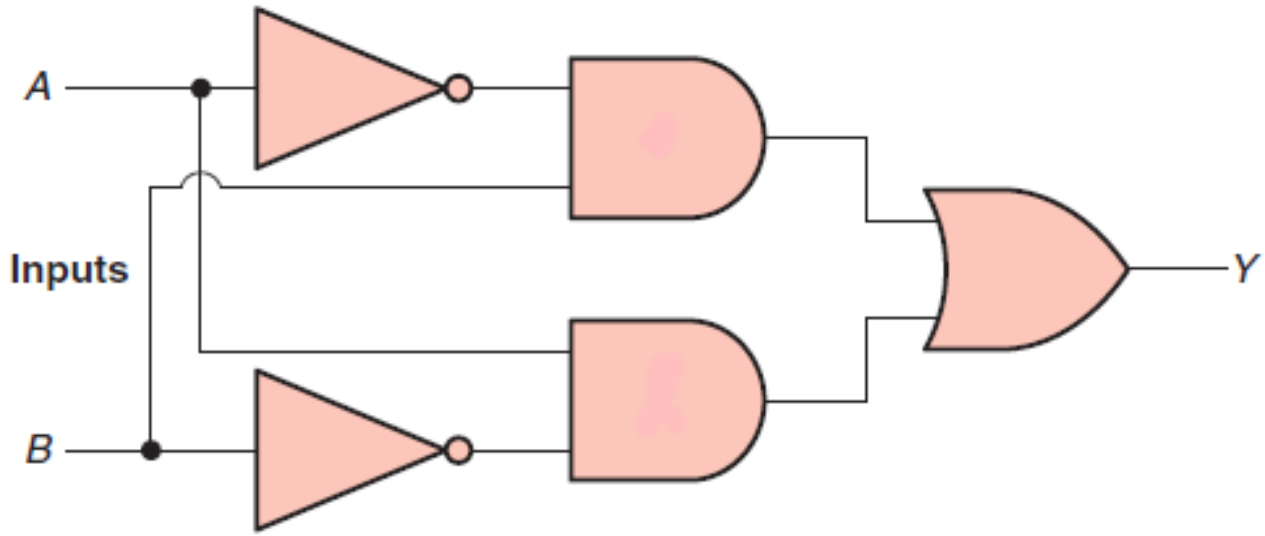
$$A \cdot (B + C) = (A \cdot B) + (A \cdot C)$$

$$A + (B \cdot C) = (A + B) \cdot (A + C)$$

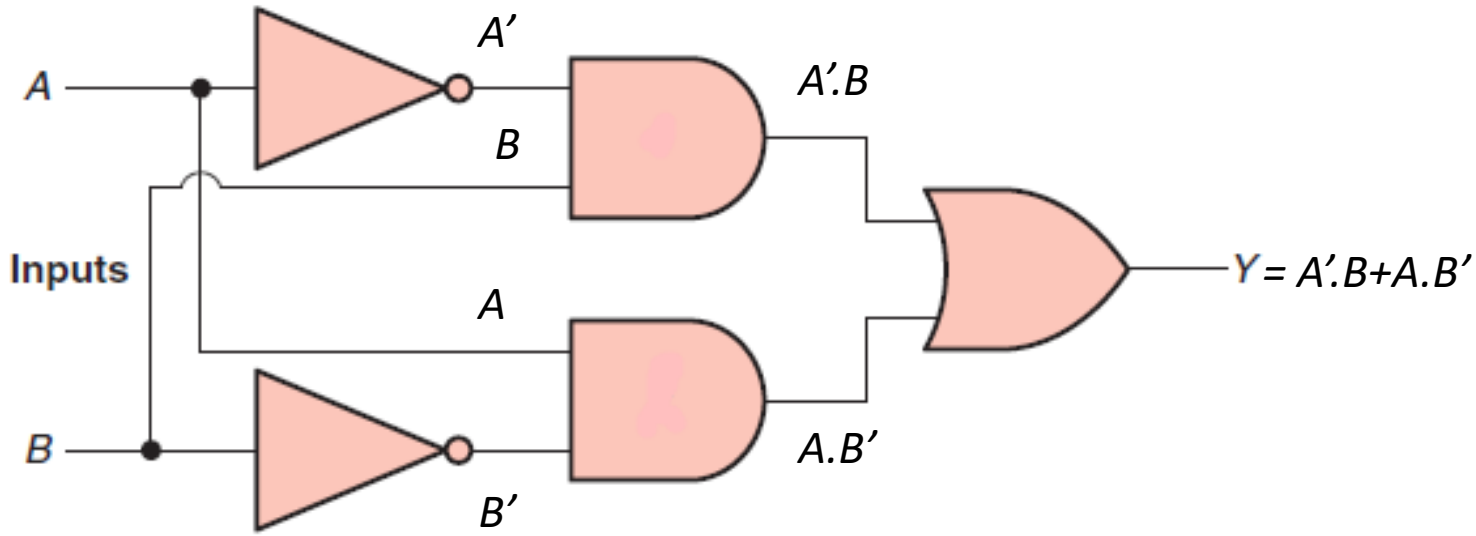
Producing the Boolean Equation for a Given Logic Gate Circuit



Producing the Boolean Equation for a Given Logic Gate Circuit



Producing the Boolean Equation for a Given Logic Gate Circuit



Chapter 4 Exercise Problem (Q5)

Write the Boolean expression and draw the gate logic diagram and typical PLC ladder logic diagram for a control system wherein a fan is to run only when all of the following conditions are met:

- Input A is OFF
- Input B is ON or input C is ON, or both B and C are ON
- Inputs D and E are both ON
- One or more of inputs F, G, or H are ON

Chapter 4 Exercise Problem (Q1)

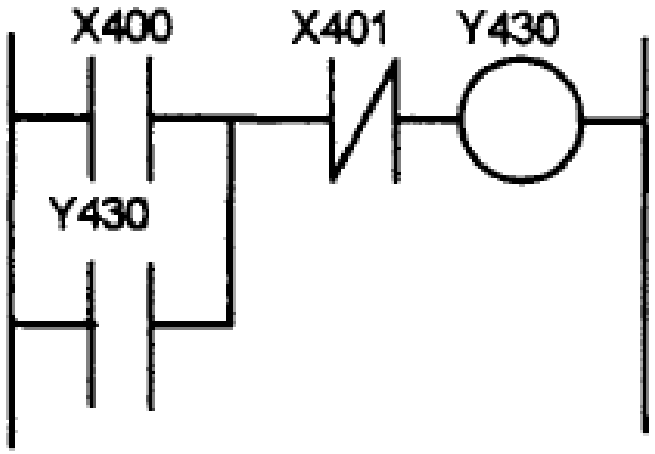
It is required to have a pilot light come on when all of the following circuit requirements are met:

- All four circuit pressure switches must be closed.
- At least two out of three circuit limit switches must be closed.
- The reset switch must not be closed.

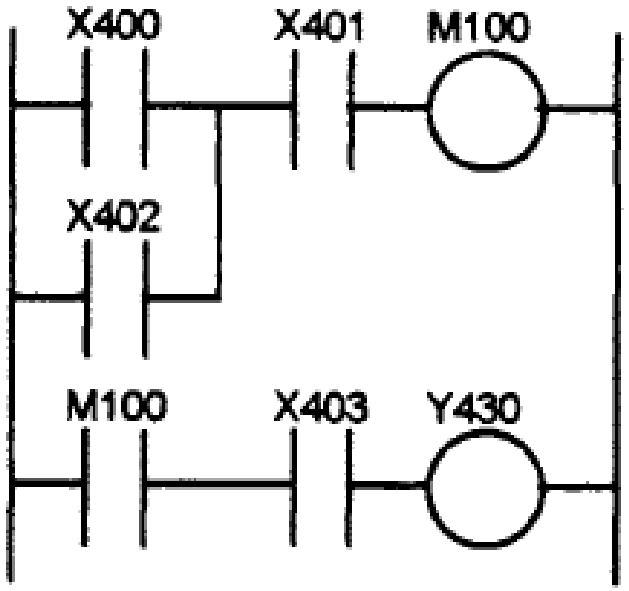
Using AND, OR, and NOT gates, design a logic circuit that will solve this hypothetical problem.

Latching

Output is used as input
Controlling remote locations



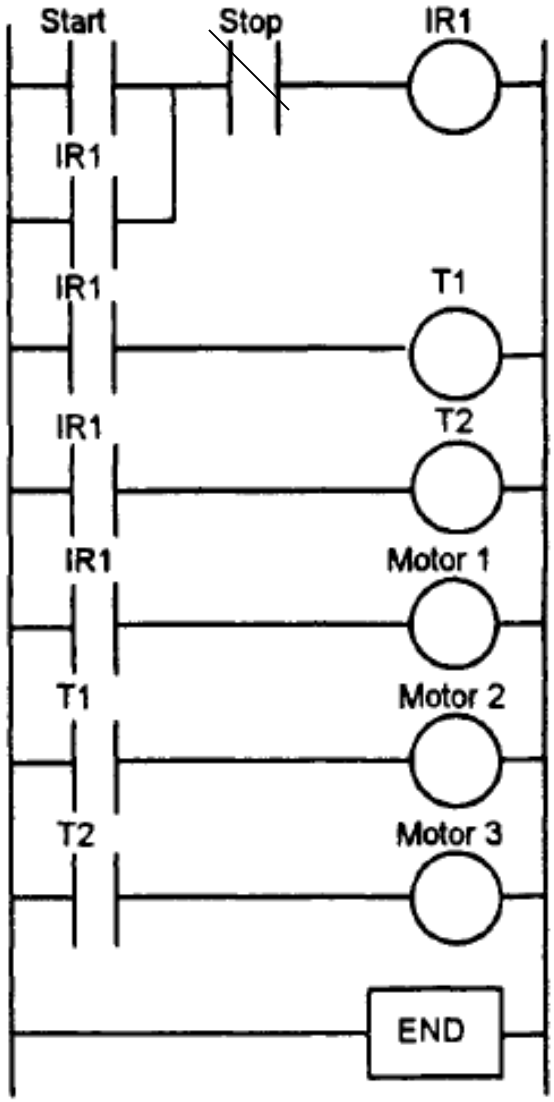
Internal Relays



Timer

- When the start button is on, internal relay is on which triggers timer 1, 2 and motor 1. The time for timer 1 is 5 seconds and timer 2 is 10 seconds. After passing 5 seconds from the start of motor 1, motor 2 starts and after 10 seconds from motor 1, motor 3 starts.
- Draw the ladder logic diagram with latching and a stop button to stop the motors

Timer


Start
Stop
IR1
IR1
IR1
T1
IR1
T2
IR1
Motor 1
T1
Motor 2
T2
Motor 3
END

Counter

- A counter allows a number of occurrences of input signals to be counted.